# SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Japanese Patent Application No. 2002-315761 filed on October 30, 2002, is hereby incorporated by reference in its entirety.

## BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device including a memory region and a method of manufacturing thereof. More particularly, the present invention relates to a method of manufacturing a semiconductor device in which a nonvolatile memory device formed in the memory region includes two charge accumulation regions for one word gate.

As one type of nonvolatile semiconductor memory device, a MONOS (Metal Oxide Nitride Oxide Semiconductor) or SONOS (Silicon Oxide Nitride Oxide Silicon) memory device is known. In this type of memory device, a gate insulating layer between a channel region and a control gate is formed of a laminate consisting of silicon oxide layers and a silicon nitride layer, and a charge is trapped in the silicon nitride layer.

A device shown in FIG. 17 is known as the MONOS nonvolatile semiconductor memory device (non-patent document: Y. Hayashi, et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 122-123).

In this MONOS memory cell 100, a word gate 14 is formed on a semiconductor substrate 10 through a gate insulating layer 12. A control gate 20 and a control gate 30 in the shape of sidewalls are disposed on each side surface of the word gate 14. An insulating layer 22 is disposed between the bottom of the control gate 20 and the semiconductor substrate 10. A side insulating layer 26 is disposed between the side surface of the control gate 20 and the word gate 14. The insulating layer 22 is disposed between the bottom of the control gate 30 and the semiconductor substrate 10.

The side insulating layer 26 is disposed between the side surface of the control gate 30 and the word gate 14. Impurity layers 16 and 18 which form either a source region or a drain region are formed in the semiconductor substrate 10 between the control gate 20 and the control gate 30 which face each other in the adjacent memory cells.

As described above, one memory cell 100 includes two MONOS memory elements, one on each side surface of the word gate 14. The two MONOS memory elements are controlled separately. Therefore, one memory cell 100 is capable of storing two bits of information.

## BRIEF SUMMARY OF THE INVENTION

The present invention may provide a semiconductor device which includes a MONOS nonvolatile memory device having two charge accumulation regions and has tolerance to deterioration during data writing/erasing, and a method of manufacturing the same.

According to one aspect of the present invention, there is provided a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns,

wherein each of the nonvolatile memory devices includes:

a word gate formed over a semiconductor layer with a gate insulating layer interposed in between;

an impurity layer formed in the semiconductor layer to form one of a source region and a drain region; and

control gates in the shape of sidewalls formed along both side surfaces of the word gate,

wherein each of the control gates includes a first control gate and a second control gate adjacent to each other,

wherein a first insulating layer formed of a first silicon oxide film, a silicon

nitride film, and a second silicon oxide film is disposed between the first control gate and the semiconductor layer, and a side insulating layer is disposed between the first control gate and the word gate;

wherein a second insulating layer formed of a silicon oxide film is disposed between the second control gate and the semiconductor layer, and

wherein the thickness of the second insulating layer is smaller than the thickness of the first insulating layer.

According to another aspect of the present invention, there is provided a method of manufacturing a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns, the method comprising the steps of:

(a) forming a gate insulating layer over a semiconductor layer,

(b) forming a first conductive layer over the gate insulating layer,

(c) forming a stopper layer over the first conductive layer,

(d) patterning the stopper layer and the first conductive layer to form a stack of layers formed of the stopper layer and the first conductive layer,

(e) forming a first insulating layer formed of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film over the entire surface of the memory region,

(f) forming a second conductive layer over the first insulating layer and anisotropically etching the second conductive layer to form a first control gate in the shape of a sidewall along both side surfaces of the first conductive layer over the semiconductor layer with the first insulating layer interposed in between,

(g) removing the silicon nitride film and the second silicon oxide film of the first insulating layer by using the first control gate as a mask to form a second insulating layer,

(h) forming a third conductive layer over the entire surface of the memory

region, and anisotropically etching the third conductive layer to form a second control gate at a location adjacent to the first control gate and over the semiconductor layer with the second insulating layer interposed in between,

(i) forming an impurity layer in the semiconductor layer to form one of a source region and a drain region,

(j) forming a third insulating layer over the entire surface of the memory region and removing the third insulating layer so as to expose the stopper layer, and

(k) removing the stopper layer, forming a fourth conductive layer, and then patterning the fourth conductive layer to form a word line.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1 is a plan view schematically showing a layout of a memory region of a semiconductor device.

FIG. 2 is a cross-sectional view schematically showing a section along the line A-A shown in FIG. 1.

FIG. 3 is an enlarged cross-sectional view showing a portion B shown in FIG. 2.

FIG. 4 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 5 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 6 is a plan view showing a step of a method of manufacturing the semiconductor device shown in FIG. 5.

FIG. 7 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 8 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 9 is a cross-sectional view showing a step of a method of manufacturing

the semiconductor device shown in FIGS. 1 to 3.

FIG. 10 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 11 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 12 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 13 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 14 is a cross-sectional view showing a step of a method of manufacturing the semiconductor device shown in FIGS. 1 to 3.

FIG. 15 is a cross-sectional view schematically showing a semiconductor device according to a second embodiment.

FIG. 16 is a cross-sectional view schematically showing a semiconductor device according to a third embodiment.

FIG. 17 is a cross-sectional view showing a conventional MONOS memory cell.

FIG. 18 is a view illustrating an erase operation of a semiconductor device of the present invention.

## DETAILED DESCRIPTION OF THE EMBODIMENT

According to one embodiment of the present invention, there is provided a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns,

wherein each of the nonvolatile memory devices includes:

a word gate formed over a semiconductor layer with a gate insulating layer interposed in between;

an impurity layer formed in the semiconductor layer to form one of a source

region and a drain region; and

control gates in the shape of sidewalls formed along both side surfaces of the word gate,

wherein each of the control gates includes a first control gate and a second control gate adjacent to each other,

wherein a first insulating layer formed of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film is disposed between the first control gate and the semiconductor layer, and a side insulating layer is disposed between the first control gate and the word gate;

wherein a second insulating layer formed of a silicon oxide film is disposed between the second control gate and the semiconductor layer, and

wherein the thickness of the second insulating layer is smaller than the thickness of the first insulating layer.

According to this semiconductor device, each of the control gates includes the first control gate and the second control gate respectively formed on the insulating layers having different thickness. Therefore, a semiconductor device in which the potential of the surface of the substrate under the control gates changes in two locations and field intensity between the control gates and the surface of the substrate is nonuniform can be provided.

This semiconductor device may have the following features.

(A) In this semiconductor device, the thickness of the silicon oxide film of the second insulating layer may be the same as the thickness of the first silicon oxide film of the first insulating layer.

(B) In this semiconductor device, at least end surfaces of the second silicon oxide film and the silicon nitride film of the first insulating layer may be covered with a charge transfer protection film. This can prevent the first insulating layer from coming in contact with the second control gate, whereby electrons stored in the first insulating

layer can be prevented from being discharged to the second control gate.

(C) In this semiconductor device, the charge transfer protection film may be one of a silicon oxide film and a silicon nitride oxide film.

According to another embodiment of the present invention, there is provided a method of manufacturing a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns, the method comprising the steps of:

(a) forming a gate insulating layer over a semiconductor layer,

(b) forming a first conductive layer over the gate insulating layer,

(c) forming a stopper layer over the first conductive layer,

(d) patterning the stopper layer and the first conductive layer to form a stack of layers formed of the stopper layer and the first conductive layer,

(e) forming a first insulating layer formed of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film over the entire surface of the memory region,

(f) forming a second conductive layer over the first insulating layer and anisotropically etching the second conductive layer to form a first control gate in the shape of a sidewall along both side surfaces of the first conductive layer over the semiconductor layer with the first insulating layer interposed in between,

(g) removing the silicon nitride film and the second silicon oxide film of the first insulating layer by using the first control gate as a mask to form a second insulating layer,

(h) forming a third conductive layer over the entire surface of the memory region, and anisotropically etching the third conductive layer to form a second control gate at a location adjacent to the first control gate and over the semiconductor layer with the second insulating layer interposed in between,

(i) forming an impurity layer in the semiconductor layer to form one of a source

region and a drain region,

(j) forming a third insulating layer over the entire surface of the memory region and removing the third insulating layer so as to expose the stopper layer, and

(k) removing the stopper layer, forming a fourth conductive layer, and then patterning the fourth conductive layer to form a word line.

According to this method of manufacturing a semiconductor device, the control gates are formed in two steps. In more detail, the first control gate is formed at first, then the second insulating layer is formed by removing the second silicon oxide film and the silicon nitride film of the first insulating layer. The second control gate is then formed over the second insulating layer. Therefore, the control gates can be formed on the insulating layers having different thickness. As a result, a semiconductor device in which field intensity between the control gates and the surface of the substrate is nonuniform can be manufactured.

This method of manufacturing a semiconductor device may have the following features.

(A) In this method of manufacturing a semiconductor device, the step (g) may include forming a charge transfer protection film so as to cover at least end surfaces of the second silicon oxide film and the silicon nitride film of the first insulating layer after forming the second insulating layer.

(B) In this method of manufacturing a semiconductor device, the step (g) may include forming a charge transfer protection film over the entire surface of the memory region after forming the second insulating layer and anisotropically etching the charge transfer protection film to form a sidewall formed of the charge transfer protection film on end surfaces of the second silicon oxide film and the silicon nitride film of the first insulating layer. According to this feature, the charge transfer protection film can be formed on the end face of the first insulating layer. As a result, a semiconductor device in which the first insulating layer is prevented from coming in contact with the

second control gate can be manufactured.

(C) In this method of manufacturing a semiconductor device, the charge transfer protection film may be formed by using a chemical vapor deposition (CVD) method.

(D) In this method of manufacturing a semiconductor device, the charge transfer protection film may be one of a silicon oxide film and a silicon nitride oxide film.

The semiconductor device and the method of manufacturing the same according to the embodiment of the present invention are described below with reference to the drawings.

1. First embodiment

1-1. Structure of device

FIG. 1 is a plan view showing a layout of a semiconductor device according to the present embodiment. The semiconductor device includes a memory region 1000 including a nonvolatile memory device.

In the memory region 1000, MONOS nonvolatile memory devices (hereinafter called "memory cells") 100 are arranged in a plurality of rows and columns in the shape of a matrix. A first block B1 and a part of other blocks B0 and B2 adjacent to the first block B1 are illustrated in the memory region 1000. The blocks B0 and B2 have a configuration which is the reverse of the configuration of the block B1.

An element isolation region 300 is formed in a part of a region between the first block B1 and the blocks B0 and B2 adjacent to the first block B1. A plurality of word lines 50 (WL) extending in the X direction (row direction) and a plurality of bit lines 60 (BL) extending in the Y direction (column direction) are provided in each block. One word line 50 is connected with a plurality of word gates 14 arranged in the X direction. The bit lines 60 are formed by impurity layers 16 and 18.

A conductive layer 40 which forms control gates 20 and 30 is formed to enclose each of the impurity layers 16 and 18. Specifically, each of the control gates 20 and 30

extends in the Y direction, and a pair of control gates 20 and 30 is connected on one end by the conductive layer extending in the X direction. The pair of control gates 20 and 30 is connected with one common contact section 200 on other end. Therefore, the conductive layer 40 has a function as the control gates of the memory cells and a function as an interconnect which connects each of the control gates arranged in the Y direction.

The single memory cell 100 includes one word gate 14, the control gates 20 and 30, and the impurity layers 16 and 18. The control gates 20 and 30 are formed on each side of the word gate 14. The impurity layers 16 and 18 are formed on the outer side of the control gates 20 and 30. The impurity layers 16 and 18 are shared by the adjacent memory cells 100.

The impurity layer 16 formed in the block B1 and the impurity layer 16 formed in the block B2, adjacent in the Y direction, are electrically connected by a contact impurity layer 400 formed in the semiconductor substrate. The contact impurity layer 400 is formed on the side of the impurity layer 16 opposite to the side of the common contact section 200 of the control gates.

A contact 350 is formed on the contact impurity layer 400. The bit line 60 formed by the impurity layer 16 is electrically connected with an upper interconnect layer through the contact 350.

The impurity layer 18 formed in the block B1 and the impurity layer 18 formed in the block B0, adjacent in the Y direction, are electrically connected by the contact impurity layer 400 on the side on which the common contact section 200 is not disposed. As shown in FIG. 1, the planar layout of a plurality of the common contact sections 200 in one block is a staggered arrangement in which the common contact sections 200 are alternately formed on opposite ends of the impurity layers 16 and the impurity layers 18. The planar layout of a plurality of the contact impurity layers 400 in one block is a staggered arrangement in which the contact impurity layers 400 are alternately formed

on opposite ends of the impurity layers 16 and the impurity layers 18.

The cross-sectional structure of the semiconductor device is described below with reference to FIGS. 2 and 3. FIG. 2 is a cross-sectional view along the line A-A shown in FIG. 1. FIG. 3 is an enlarged cross-sectional view showing a portion B shown in FIG. 2.

In the memory region 1000, the memory cell 100 includes the word gate 14, the impurity layers 16 and 18, and the control gates 20 and 30. The word gate 14 is formed over the semiconductor substrate 10 through a gate insulating layer 12. The impurity layers 16 and 18 are formed in the semiconductor substrate 10. Each of the impurity layers becomes either a source region or a drain region. A silicide layer 92 is formed on the impurity layers 16 and 18.

The control gates 20 and 30 are formed along each side of the word gate 14. The control gate 20 includes a first control gate 20a and a second control gate 20b which are in contact with each other. The first control gate 20a is formed over the semiconductor substrate 10 through a first insulating layer 22, and is formed on one side surface of the word gate 14 through a side insulating layer 26. The second control gate 20b is formed over the semiconductor substrate 10 through a second insulating layer 24. The control gate 30 includes a first control gate 30a and a second control gate 30b.

The first insulating layer 22 is an ONO film. In more detail, the first insulating layer 22 is a stacked film of a bottom silicon oxide layer (first silicon oxide layer) 22a, a silicon nitride layer 22b, and a top silicon oxide layer (second silicon oxide layer) 22c.

The second insulating layer 24 is formed of a silicon oxide film 24a. The silicon oxide film 24a is formed in the step as the first silicon oxide layer 22a of the first insulating layer 22, and has a thickness approximately the same as the thickness of the first silicon oxide layer 22a.

The first silicon oxide layer 22a forms a potential barrier between a channel region and a charge accumulation region. The silicon nitride layer 22b functions as the

charge accumulation region which traps carriers (electrons, for example). The second silicon oxide layer 22c forms a potential barrier between the control gate and the charge accumulation region.

The side insulating layer 26 is an ONO film. In more detail, the side insulating layer 26 is a stacked film of a first silicon oxide layer 26a, a silicon nitride layer 26b, and a second silicon oxide layer 26c. The side insulating layer 26 electrically isolates the word gate 14 from each of the control gates 20 and 30. At least the upper end of the first silicon oxide layer 26a of the side insulating layer 26 is located at a position higher than the upper ends of the control gates 20 and 30 with respect to the semiconductor substrate 10 in order to prevent occurrence of short circuits between the word gate 14 and the control gates 20 and 30.

The side insulating layer 26 and the first insulating layer 22 are formed in the same deposition step and have the same layer structure.

The surfaces of the control gates 20 and 30 are covered with a sidewall insulating layer 152.

A buried insulating layer 70 is formed between the adjacent control gates 20 and 30 in the adjacent memory cells 100. The buried insulating layer 70 covers the control gates 20 and 30 so that at least the control gates 20 and 30 are not exposed. The upper surface of the buried insulating layer 70 is located at a position higher than the upper surface of the word gate 14 with respect to the semiconductor substrate 10. The control gates 20 and 30 can be electrically isolated from the word gate 14 and the word line 50 more reliably by forming the buried insulating layer 70 in this manner.

As shown in FIG. 2, the word line 50 is formed on the word gate 14.

In the semiconductor device of the present embodiment, the control gates 20 and 30 are respectively formed of the first control gates 20a and 30a and the second control gates 20b and 30b which are formed on the insulating layers having different thickness. Therefore, the potential of the surface of the substrate under the control gates 20 and 30

changes in two stages, whereby the field intensity has peaks at three locations including the boundary between the word gate 14 and the control gates 20 and 30, the boundary between the first control gates 20a and 30a and the second control gates 20b and 30b, and the edge of the impurity region. This contributes to the following advantages relating to the data write/erase operation of the memory cell 100.

The data write operation is described below. In the case of writing data in the memory cell 100, electrons transferred from the impurity region 16 are provided with energy at the boundary between the word gate 14 and the control gate 30. The electrons are then provided with energy at the boundary between the first control gate 30a and the second control gate 30b to become hot electrons. The hot electrons are injected and trapped in the first insulating layer 22 near the region at which the thickness of the insulating layers differ.

In the semiconductor device of the present embodiment, the electron injection locations are distributed around the boundary between the first control gate 30a and the second control gate 30b. However, since the second insulating layer 24 formed of the silicon oxide film is present under the second control gate 30b, a charge escapes through the control gate 30. As a result, electrons trapped on the side of the first control gate 30a remain.

The data erase operation is described below with reference to FIG. 18. FIG. 18 is a band diagram in which the vertical axis indicates electron potential energy and the horizontal axis indicates a real-space coordinate. FIG. 18 shows a state at the edge of the impurity layer 18, specifically, the pn junction.

A high positive voltage is applied to the impurity layer 18, and a negative voltage is applied to the control gate 30. As a result, the electron potential energy is decreased in the impurity layer 18 which is an n-type region (electron potential energy in the n-type region shifts in the direction indicated by an arrow in FIG. 18). Since the thickness of the depletion layer is as small as several nanometers in a high concentration

pn junction, electrons in the p-type valence band can move into the n-type conduction band by a tunneling effect. Specifically, holes are generated near the edge of the impurity layer 18 which is the p-type region accompanying transfer of electrons. This means that a hole storage layer is formed near the edge of the impurity layer.

The electric field between the second control gate 30b formed over the second insulating layer 24 and the surface of the substrate and the electric field between the first control gate 30a formed over the first insulating layer 22 and the surface of the substrate are described below. Since the hole storage layer is formed in the second insulating layer 24, carrier conductivity of the second insulating layer 24 is high. Therefore, the electric field in the horizontal direction (gate length direction) is relatively small. Since the second insulating layer 24 has a thickness smaller than that of the first insulating layer 22, the electric field in the vertical direction is relatively large. Therefore, holes generated near the edge of the impurity layer 18 cannot enter the second insulating layer 24.

In the first insulating layer 22, the electric field in the horizontal direction is relatively large and the electric field in the vertical direction is relatively small. Therefore, holes generated near the edge of the impurity layer 18 are provided with a large amount of energy at the boundary between the second insulating layer 24 and the first insulating layer 22, and enter the charge accumulation film. Specifically, holes are injected at a location near the region at which the thickness of the charge accumulation films differs, and data is erased at this location.

The location at which the electrons are injected during writing can be allowed to coincide with the location at which the holes are injected during erasing in this manner. As a result, a nonvolatile memory device which does not deteriorate even if the write/erase cycles are repeated can be realized.

1-2. Method of manufacturing semiconductor device

A method of manufacturing the semiconductor device of the present embodiment is described below with reference to FIGS. 4 to 14. Each cross-sectional view corresponds to the section along the line A-A shown in FIG. 1. In FIGS. 4 to 14, sections substantially the same as the sections shown in FIGS. 1 to 3 are indicated by the same symbols. The description of these sections is omitted.

(1) The element isolation region 300 (see FIG. 1) is formed on the surface of the semiconductor substrate 10 by using a trench isolation method. p-type impurities are then implanted as channel doping. The n-type contact impurity layer 400 (see FIG. 1) is formed in the semiconductor substrate 10 by ion implantation.

As shown in FIG. 4, an insulating layer 120 which becomes the gate insulating layer is formed on the surface of the semiconductor substrate 10. A gate layer (first conductive layer) 140 which becomes the word gate 14 is deposited on the insulating layer 120. The gate layer 140 is formed of doped polysilicon. A stopper layer S100 used in a CMP step described later is formed on the gate layer 140. The stopper layer S100 is formed of a silicon nitride layer.

(2) A resist layer (not shown) is formed. The stopper layer S100 is patterned by using the resist layer as a mask. The gate layer 140 is etched using the patterned stopper layer S100 as a mask. As shown in FIG. 5, the gate layer 140 is patterned and becomes a gate layer (word gate) 140a.

FIG. 6 is a plan view showing the state after patterning. Openings 160 and 180 are formed in the laminate consisting of the gate layer 140a and the stopper layer S100 in the memory region 1000 by this patterning. The openings 160 and 180 approximately correspond to regions in which the impurity layers 16 and 18 are formed by ion implantation described later. The side insulating layer and the control gate are formed along the side surfaces of the openings 160 and 180 in a step described later.

(3) The surface of the semiconductor substrate 10 is washed by using diluted fluoric acid. This allows the exposed insulating layer 120 to be removed and the gate

insulating layer 12 to remain. As shown in FIG. 7, a first silicon oxide film 220a is deposited by using a thermal oxidation method. The first silicon oxide film 220a is formed on the exposed surfaces of the semiconductor substrate 10 and the gate layer 140a. The first silicon oxide film 220a may be formed by using a chemical vapor deposition (CVD) method.

The first silicon oxide film 220a is subjected to an annealing treatment. The annealing treatment is performed in an atmosphere containing $NH_3$ gas. This pretreatment enables a silicon nitride film 220b to be uniformly deposited on the first silicon oxide film 220a. The silicon nitride film 220b is deposited by using a CVD method.

A second silicon oxide film 220c is deposited by using a CVD method or a high temperature oxidation (HTO) method, for example. The second silicon oxide film 220c may be deposited by using an in-situ steam generation (ISSG) treatment. A dense film is deposited by using the ISSG treatment. In the case of depositing the second silicon oxide film 220c by using the ISSG treatment, an annealing treatment for making the ONO film dense as described layer may be omitted.

In the above step, interfacial contamination due to removal from a furnace can be prevented by depositing the silicon nitride film 220b and the second silicon oxide film 220c in the same furnace. This enables a uniform ONO film to be formed, whereby the memory cell 100 having stable electrical characteristics can be obtained.

In the present embodiment, an ONO film 220 becomes the first insulating layer 22, the second insulating layer 24, and the side insulating layer 26 (see FIGS. 2 and 3) by patterning described later.

(4) As shown in FIG. 8, a doped polysilicon layer (second conductive layer) 230 is formed on the second silicon oxide film 220c. The doped polysilicon layer 230 is etched in a step described later and becomes the conductive layer 40 (see FIG. 1) which forms the control gates 20 and 30.

(5) As shown in FIG. 9, the entire surface of the doped polysilicon layer 230 is anisotropically etched. This allows a sidewall-shaped conductive layer 232 to be formed along the side surfaces of the openings 160 and 180 (see FIG. 6) in the memory region 1000. The sidewall-shaped conductive layer 232 is etched in a step described later and becomes the first control gates 20a and 30a.

(6) As shown in FIG. 10, a part of the ONO film 220 is removed by using the sidewall-shaped conductive layer 232 as a mask. In more detail, the second silicon oxide film 220c and the silicon nitride film 220b are removed. These films may be removed by wet etching using diluted fluoric acid, or dry etching. This allows the first insulating layer 22 formed of the ONO film to remain under the first control gates 20a and 30a.

(7) A doped polysilicon layer (not shown) is formed over the entire surface. The entire surface of the doped polysilicon layer is anisotropically dry-etched. This allows the first control gates 20a and 30a to be formed by decreasing the height of the sidewall-shaped conductive layer 232, and the second control gates 20b and 30b to be formed on the stacked film of the second insulating layer 24 formed of the first silicon oxide layer 24a, as shown in FIG. 11.

Since the first control gates 20a and 30a and the second control gates 20b and 30b are formed in the same step, the heights of the first control gates 20a and 30a and the second control gates 20b and 30b can be easily made uniform. The surfaces of the control gates 20 and 30 are gently sloped by isotropic etching. This allows the exposed second silicon oxide layer 24a to be removed.

(8) An insulating layer (not shown) such as silicon oxide or silicon nitride oxide is formed over the entire surface of the memory region 1000. As shown in FIG. 12, the sidewall insulating layer 152 is formed to cover the control gates 20 and 30 by anisotropically etching the insulating layer. The insulating layer deposited in a region in which the silicide layer is formed in a step described later is removed by this etching,

whereby the semiconductor substrate 10 is exposed.

As shown in FIG. 12, the impurity layers 16 and 18 are formed in the semiconductor substrate 10 by ion implantation with n-type impurities.

A metal for forming a silicide is deposited over the entire surface. As examples of the metal for forming a silicide, titanium and cobalt can be given. The metal formed on the semiconductor substrate 10 is subjected to a silicidation reaction, thereby forming the silicide layer 92 on the exposed surface of the semiconductor substrate 10. A third insulating layer 270 such as silicon oxide or silicon nitride oxide is formed over the entire surface of the memory region 1000. The third insulating layer 270 is formed to cover the stopper layer S100.

(9) As shown in FIG. 13, the third insulating layer 270 is planarized by grinding the third insulating layer 270 using a CMP method until the stopper layer S100 is exposed. This grinding allows the buried insulating layer 70 to remain between the control gates 20 and 30 which face each other.

(10) The stopper layer S100 is removed by using thermal phosphoric acid. As a result, at least the upper surface of the gate layer 140a is exposed, and an opening 170 is formed in the third insulating layer 270. Specifically, the opening 170 is a region which is formed by removing the stopper layer S100 and is located on the gate layer 140a.

(11) A doped polysilicon layer (not shown) is deposited over the entire surface. A patterned resist layer (not shown) is formed on the doped polysilicon layer. The doped polysilicon layer is patterned by using the resist layer as a mask, whereby the word line 50 (see FIG. 2) is formed.

The gate layer 140a is etched by using the resist layer as a mask. This etching allows the gate layer 140a to be removed in the region in which the word line 50 is not formed. As a result, the word gates 14 (see FIG. 1) arranged in an array are formed. The region in which the gate layer 140a is removed corresponds to the region in which

the p-type impurity layer (element isolation impurity layer) 15 is formed later (see FIG. 1).

In this etching step, the control gates 20 and 30 remain without being etched since the control gates 20 and 30 are covered with the buried insulating layer 70.

The entire surface of the semiconductor substrate 10 is doped with p-type impurities. This allows the p-type impurity layer (element isolation impurity layer) 15 (see FIG. 1) to be formed in the region between the word gates 14 adjacent in the Y direction. The nonvolatile semiconductor memory devices 100 can be isolated more reliably by the p-type impurity layer 15.

The semiconductor device shown in FIGS. 1 to 3 is manufactured by these steps.

An advantage of this manufacturing method is as follows.

The control gates 20 and 30 are formed in the step in two stages. In more detail, after forming the first control gates 20a and 30a, the second silicon oxide layer 220c and the silicon nitride film 220b of the ONO film 220 are removed, and the second control gates 20b and 30b are formed. Therefore, the control gates 20 and 30 can be formed on the insulating layers having different thickness. As a result, a semiconductor device in which field intensity between the control gates 20 and 30 and the surface of the substrate is nonuniform can be manufactured.

## 2. Second embodiment

A second embodiment of the present invention is described below. The following description merely illustrates features differing from the features of the first embodiment.

### 2-1. Structure of device

FIG. 15 is a cross-sectional view schematically showing a semiconductor device according to the second embodiment. FIG. 15 is a cross-sectional view showing a

portion corresponding to FIG. 3 in the first embodiment.

In the semiconductor device according to the second embodiment, the second control gate 30b is formed on the first control gate 30a through a charge transfer protection film 42 and is formed on the semiconductor substrate 10 through the second insulating layer 24 and the charge transfer protection film 42, as shown in FIG. 15. There are no specific limitations to the charge transfer protection film 42 insofar as the charge transfer protection film 42 has a function of preventing a charge stored in the silicon nitride film 22b from being discharged to the second control gate 30b. For example, a silicon oxide film may be used as the charge transfer protection film 42. There are no specific limitations to the thickness of the charge transfer protection film 42 insofar as the charge transfer protection film 42 has a thickness which prevents the end face of the silicon nitride film 22b of the first insulating layer 22 from being exposed. The charge transfer protection film 42 is formed by using a CVD method. The charge transfer protection film 42 is formed to cover the second insulating layer 24 and the first control gate 30a.

2-2. Method of manufacturing semiconductor device

A method of manufacturing the semiconductor device according to the second embodiment is described below. In the following description, steps the same as the steps in the first embodiment are described by using the drawings common to the first embodiment.

The steps (1) to (5) are performed in the same manner as in the first embodiment.

(6) As shown in FIG. 9, the second silicon oxide film 220c and the silicon nitride film 220b of the ONO film 220 are removed by using the sidewall-shaped conductive layer 232 as a mask. This allows the first insulating layer 22 formed of the ONO film to remain under the first control gates 20a and 30a. In more detail, the

etching may be performed by wet etching using diluted fluoric acid or dry etching. The charge transfer protection film 42 (see FIG. 15) is formed over the entire surface. A silicon oxide film or a silicon nitride oxide film may be formed as the charge transfer protection film 42.

The charge transfer protection film 42 is formed by using a CVD method, for example. In this case, the charge transfer protection film 42 is formed to cover the end face of the first insulating layer 22, the first control gate 30a, and the side insulating layer 26 in a region in which the side insulating layer 26 is not in contact with the first control gate 30a.

(7) A doped polysilicon layer (not shown) is formed over the entire surface. The entire surface of the doped polysilicon layer is anisotropically dry-etched. This allows the first control gates 20a and 30a to be formed by decreasing the height of the sidewall-shaped conductive layer 232, and the second control gates 20b and 30b to be formed on the stacked film of the charge transfer protection film 42 and the second insulating layer 24 formed of the silicon oxide layer 24a, as shown in FIG. 10.

The steps (8) to (11) are performed in the same manner as in the first embodiment to obtain the semiconductor device shown in FIG. 15.

According to the method of manufacturing the semiconductor device of the second embodiment, the charge transfer protection film 42 is formed to cover at least the end face of the first insulating layer 22. Therefore, the end face of the silicon nitride film 22b of the first insulating layer 22 can be prevented from coming in contact with the second control gates 20b and 30b. This prevents electrons stored in the silicon nitride film 22b from being discharged to the second control gates 20b and 30b, whereby a semiconductor device having improved charge retention characteristics can be provided.

3. Third embodiment

A third embodiment of the present invention is described below. The following description merely illustrates features differing from the features of the first embodiment.

3-1. Structure of device

FIG. 16 is a cross-sectional view schematically showing a semiconductor device according to the third embodiment. FIG. 16 is a cross-sectional view showing a portion corresponding to FIG. 3 in the first embodiment.

In the semiconductor device shown in FIG. 16, the second control gate 30b is formed to be adjacent to the first control gate 30a and is formed on the semiconductor substrate 10 through the second insulating layer 24. A sidewall 44 consisting of a charge transfer protection film is formed on the end surfaces of the second silicon oxide film 22c and the silicon nitride film 22b of the first insulating layer 22. The charge transfer protection film which forms the sidewall 44 is not limited insofar as the charge transfer protection film is a film having the same function as in the second embodiment. For example, a silicon oxide film may be used as the charge transfer protection film.

3-2. Method of manufacturing semiconductor device

A method of manufacturing the semiconductor device according to the third embodiment is described below. In the following description, steps the same as the steps in the first embodiment are described by using the drawings common to the first embodiment.

The steps (1) to (5) are performed in the same manner as in the first embodiment.

(6) As shown in FIG. 9, the second silicon oxide film 220c and the silicon nitride film 220b of the ONO film 220 are removed by using the sidewall-shaped conductive layer 232 as a mask. This allows the first insulating layer 22 formed of the

ONO film to remain under the first control gates 20a and 30a. In more detail, the etching may be performed by wet etching using diluted fluoric acid or dry etching. The charge transfer protection film (not shown) is formed over the entire surface. A silicon oxide film or a silicon nitride oxide film may be formed as the charge transfer protection film. The charge transfer protection film is formed by using a CVD method, for example.

The charge transfer protection film formed over the entire surface is anisotropically dry-etched, whereby the sidewall 44 consisting of the charge transfer protection film is formed on the end surfaces of the second silicon oxide layer 22c and the silicon nitride film 22b of the first insulating layer 22.

The steps (7) to (11) are performed in the same manner as in the first embodiment to obtain the semiconductor device shown in FIG. 16.

According to the method of manufacturing the semiconductor device of the third embodiment, the charge transfer protection film 44 is formed to cover at least the end surfaces of the silicon nitride film 22b and the second silicon oxide layer 22c of the first insulating layer 22. Therefore, the end face of the silicon nitride film 22b of the first insulating layer 22 can be prevented from coming in contact with the second control gates 20b and 30b. This prevents electrons stored in the silicon nitride film 22b from being discharged to the second control gates 20b and 30b, whereby a semiconductor device having improved charge retention characteristics can be provided.

The present invention is not limited to the above-described embodiments. Various modifications and variations are possible within the scope of the present invention. For example, a bulk semiconductor substrate is used as the semiconductor layer in the above embodiments. However, a semiconductor layer of an SOI substrate may be used. In the above-described embodiments, these semiconductor layers may be referred to as the "semiconductor layer".